

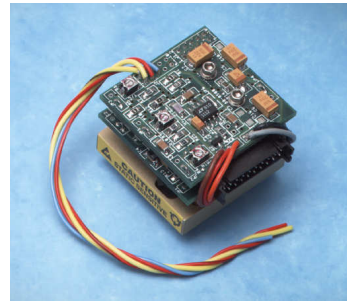


MICRO LAMBDA WIRELESS, INC.

YIG DEVICE (RS SERIES) DRIVERS SERIAL REMOTE SERIES FOR ELECTROMAGNETIC DEVICES .5-50 GHz

FEATURES

- All Electromagnetic Oscillators and Filters
- Compensation for Temperature Drift
- Voltage Regulators for Improved Stability
- 16 Bit Tuning Resolution
- Remote Device/Driver Location



DESCRIPTION

All Micro Lambda Electromagnetic YIG Devices are available with remotely located serial driver circuits. These drivers eliminate the need for customers to design or develop their own circuits and sophisticated test and alignment procedures. These remote drivers can be aligned at Micro Lambda's factory to ensure peak performance. Alignment and compensation with the particular YIG Device can be maximized down to the component level.

All drivers in this series provide input voltage regulators, reverse voltage/dataline protection and compensation circuits to improve frequency drift. All voltages required by the YIG Device, except the heater inputs are supplied by the voltage regulators.

| COMMERCIAL SERIAL DRIVERS | .5-50 GHz YIG DEVICE, SERIAL SERIES |
|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DRIVER INPUT & RESPONSE | SPECIFICATION (0 to + 65 deg. C) |
| Tuning Command | Start Word (all 0's) = Lowest Frequency Stop Word (all 1's) = Highest Frequency |
| Tuning Resolution | 16 BIT Positive Logic (Fmax-Fmin)/65,535 Resolution |
| Frequency Accuracy (Note 1) (excluding hysteresis) | YIG Device Accuracy +2 MHz |
| Tuning Speed | 5 mSec for 1 GHz step to within +/- 10 MHz. |
| Main Driver Inputs | |
| Supply Voltage & Current (Note 2) | Device Tuning Current + 100 mA, Max. |
| +15 V +/- .5 V | 100 mA, (Plus Oscillator -5 Vdc Current if any) Max. |
| -15 V +/- .5 V | |
| Supply Voltage Pushing | +/- .2%MHz Max. @ .5Vdc (2-3000 kHz) |
| Supply Voltage Ripple | 10 mV Ripple Pk-Pk from 2 kHz to 3 MHz |
| Ground | Chassis Ground |
| YIG Heater Voltage & Current (Note 3) | 750 mA surge for 2 seconds, 150 mA steady state |
| +24 Vdc ±4 Vdc | Polarity independent : ±12 Vdc or ±15 Vdc acceptable |
| Digital Interface | The MLWI digital driver interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The 3-wire serial interface will operate in a 5V or 3.3V logic system. The chip-select input (CSELECTn) frames the serial data loading at the data input pin (DATA). Immediately following CSELECTn's high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial-clock input (CLOCK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on CSELECTn's low-to-high transition (Figure 2). Note that if CSELECTn does not remain low during the entire 16 CLOCK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word. |
| Power-On Reset | The MLWI digital driver has a power-on reset circuit to set the DAC's output to OV(F-min) in unipolar mode when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss. |

Note 1: Accuracy Includes Temperature Drift & Linearity.
 2. Some YIG Devices require higher voltages - Check with factory.
 3. See particular YIG Device specification for heater current requirements.

SERIAL REMOTE SERIES (RS-SERIES) — CONT.

Serial Interface Timing Diagrams

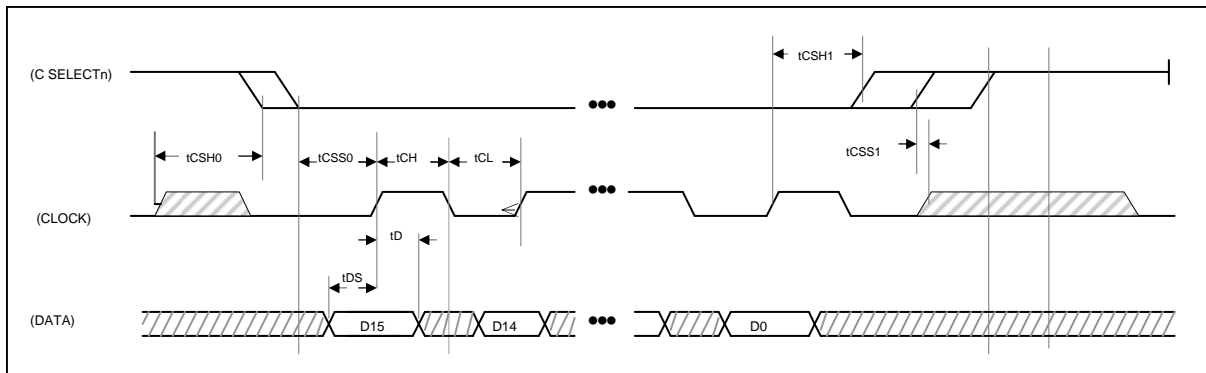


Figure 1. Timing Diagram

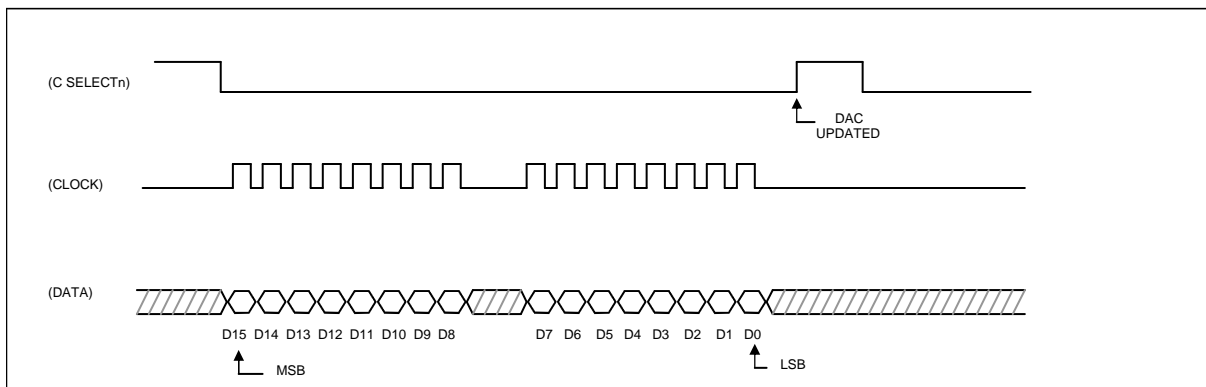


Figure 2. 3-Wire Interface Timing Diagram

TIMING CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--------|------------|-----|-----|-----|-------|
| CLOCK Frequency | fCLK | | | | 10 | MHz |
| CLOCK Pulse Width High | tCH | | 45 | | | ns |
| CLOCK Pulse Width Low | tCL | | 45 | | | ns |
| CSn Low to CLOCK High Setup | tCSS0 | | 45 | | | ns |
| CSn High to CLOCK High Setup | tCSS1 | | 45 | | | ns |
| CLOCK High to CSn Low Hold | tCSH0 | | 30 | | | ns |
| CLOCK High to CSn High Hold | tCSH1 | | 45 | | | ns |
| DATA to CLOCK High Setup | tDS | | 40 | | | ns |
| DATA to CLOCK High Hold | tDH | | 0 | | | ns |
| VDD High to CSn Low (power-up delay) | | | | 20 | | μs |

